

Roll.No.

24UACT4006

SHRIMATHI DEVKUNVAR NANALAL BHATT VAISHNAV COLLEGE FOR WOMEN  
(AUTONOMOUS)

(Affiliated to the University of Madras and Re-accredited with 'A+' Grade by NAAC)  
Chromepet, Chennai - 600 044.

B.C.A. - END SEMESTER EXAMINATIONS - NOVEMBER 2025  
SEMESTER - IV

**24UACT4006 - Computer Architecture**

Total Duration : 2 Hrs.30 Mins.

Total Marks : 60

### Section B

Answer any **SIX** questions ( $6 \times 5 = 30$  Marks)

1. Explain the operation of a 4-to-16 decoder with a neat diagram.
2. Describe the different types of micro-operations in a digital computer and give one example for each.
3. Discuss the organization of a microprogrammed control unit with the help of a block diagram.
4. Explain various addressing modes used in computer architecture with suitable examples.
5. Define pipelining. Describe the different stages of an instruction pipeline.
6. Explain the differences between SIMD and MIMD architectures with examples.
7. Describe the modes of data transfer between CPU and I/O devices.
8. Write short notes on (i) Main memory (ii)Auxiliary memory (iii) Associative memory.

### Section C

Answer any **THREE** questions ( $3 \times 10 = 30$  Marks)

9. Design and explain a 4-bit arithmetic logic shift unit (ALSU).Describe how arithmetic, logic, and shift micro-operations are performed using common hardware.
10. With a neat diagram, explain the organization of a Central Processing Unit.Discuss instruction format, addressing modes, and how program control is achieved during execution.
11. Analyze the concept of parallel processing and instruction pipelining.Compare vector processors and array processors, highlighting their advantages and limitations.

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12. Examine the working of an interrupt system in a computer. Explain priority interrupt handling, DMA, and serial communication with suitable block diagrams.
13. Evaluate the different levels of memory hierarchy in a computer system. Discuss the principles of cache mapping techniques and virtual memory implementation.

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